REMARKS

Claims 1-30 are in the application as filed. Claims 1-30 were subject to a restriction requirement.

RESTRICTION

Claims 1-30 were subject to restriction. Claims 1-5, 22-16 and 21-25 were elected. The patent office has further noted the following species and has requested that applicant elect one of the below species to prosecute herein:

Species 1 Fig. 1-4 stacked capacitor
Species 2 Fig. 5A-5I
Species 3 Fig. 6A-6D
Species 4 Fig. 7A-7B
Species 5 Fig. 8A-10B

Applicant, though his attorney Barbara C. Siegell, has provisionally elected species 1, Claims 1-5. This election is affirmed herein. Claims 6-30 are listed as withdrawn from consideration in the present case and have been marked accordingly.

REJECTION UNDER 35 USC 102(e)

Claims 1-5 were rejected under 102(e) over Nakano et al. (6,785,121).

Regarding Claim 1, as shown in Figure 1, Nagano was cited as showing a printed wiring board that is similar to that claimed by applicants in Claims 1-5.

Applicant respectfully disagrees that his invention is anticipated under 35 USC 102(e) by the Nagano drawing, for the following reasons. US 6,785,121 B2 teaches a multilayer ceramic capacitor. Multilayer ceramic capacitors are well known and many of them are constructed in a similar manner to those in the drawing in '121. Multilayer ceramic capacitors similar to those described in US 6,785,121 B2 are formed to create a single capacitor entity that is mounted on a printed wiring board, typically as a surface mounted component. The claims of US 6,785,121 B2 are related to the character of the dielectric.

US 6,785,121 B2 claims a multilayer ceramic capacitor while the present application claims a printed wiring board. The capacitors of EL-0497 are a multiplicity of fired-on foil capacitors formed on individual layers that are used as embedded capacitor elements within the substrate of a printed wiring board. The capacitor elements of the present application are formed and then incorporated into an organic layer of the printed wiring board substrate. An individual fired-on-foil capacitor may be constructed with multiple ceramic and conductor

layers before being incorporated into a layer of the printed wiring board. Once the fired-on-foil capacitors are made and incorporated into a layer of the printed wiring board, multiples of these layers may be stacked together with other layers to form the multilayer printed wiring board. Once these layers are stacked and the printed wiring board is formed, various structures of the internal layers may be electrically connected by conductive through-hole vias or microvias. Applicant asserts that US 6,785,121 B2 does not teach embedding ceramic capacitors within the organic medium of a printed wiring board. US 6,785,121 B2 also does not teach creation of fired-on-foil capacitors.

As noted above, while the drawings of US 6,785,121 B2 show a typical stacked multilayer ceramic capacitor construction where electrodes are connected in parallel, this technology is already well known in the making of multilayer ceramic capacitors and is not what is claimed either in US 6,785,121 B2 or what is claimed in the present application.

The present application teaches the making of fired-on-foil capacitors which are then incorporated into the organic layers of a printed wiring board to be used as embedded passive elements which are subsequently connected to the circuitry of a printed wiring board by use of conductive vias. The connecting of capacitors in parallel is known and this is not what applicant seeks protection for. The connecting of formed-on-foil capacitors within the layers of a printed wiring board to create embedded capacitors is what applicant asserts is novel.

In view of the above discussion and the amendment to the claims, allowance of Claims 1-5 is respectfully requested.

If anything further is needed to advance the allowance of this application the examiner is urged to contact applicants' attorney at the telephone number below.

Respectfully submitted,

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